EXHIBIT 9

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| 1 | UNITED STATES PATENT AND TRADEMARK OFFICE | |
| 2 | BEFORE THE PATENT TRIAL AND APPEAL BOARD | |
| 3 | | |
| 4 | SAMSUNG ELECTRONICS CO., LTD., | |
| 5 | Petitioner, | |
| 6 | v. | |
| 7 | NETLIST, INC., | |
| 8 | Patent Owner, | |
| 9 | | |
| 10 | Case No. IPR2022-00615 | |
| 11 | Patent No. 7,619,912 | |
| 12 | | |
| 13 | | |
| 14 | | |
| 15 | | |
| 16 | REMOTE VIDEOTAPED DEPOSITION BY VIRTUAL ZOOM OF | |
| 17 | ANDREW WOLFE, PH.D. | |
| 18 | WEDNESDAY, JANUARY 4, 2023 | |
| 19 | | |
| 20 | | |
| 21 | Reported by: | |
| 22 | Ashala Tylor, CSR #2436, CLR, CRR, RPR | |
| 23 | JOB NO. 5621734 | |
| 24 | | |
| 25 | PAGES 1 - 233 | |
| | | |
| | Page 1 | |

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| 3101 | |
|---|---|
| 1 something that could be implemented as a 10:52 | 1 MS. ZHONG: We can take a break. How long 10:56 |
| 2 point-to-point link, but there's also a discussion 10:52 | 2 do you want it to be? 10:56 |
| 3 of other kinds of links as well. 10:52 | Why don't we get off the record and then 10:57 |
| 4 MR. CHANDLER: We have been going about 10:52 | 4 we can discuss how long the breaks needs to be. 10:57 |
| 5 two hours. Whenever you are at a good breaking 10:53 | 5 MR. CHANDLER: Okay. 10:57 |
| 6 point, it might be a nice time for a break. 10:53 | 6 (Recess.) 11:08 |
| 7 MS. ZHONG: Sure. 10:53 | 7 (Off record: 10:57 a.m.) 11:08 |
| 8 Q. Why don't we take a look at your 10:53 | 8 (On record: 11:16 a.m.) 11:08 |
| 9 declaration, Exhibit 1003, page 77, paragraph 133. 10:53 | 9 MS. ZHONG: We can go back on the record. 11:16 |
| 10 Are you there? 10:53 | 10 Q. Dr. Wolfe, can you go back to your 11:17 |
| 11 A. Yes. 10:53 | 11 declaration, Exhibit 1003, page 93? |
| 12 Q. So for the specific citation that you 10:53 | 12 A. Okay. 11:17 |
| 13 quoted here, which I believe we discussed earlier, 10:53 | 13 Q. Do you see Table 10, the command truth 11:17 |
| 14 that is a distinct signaling scheme from the JEDEC 10:54 | 14 table? 11:17 |
| 15 compliant signaling scheme; is that correct? 10:54 | 15 A. Yes. 11:17 |
| 16 MR. CHANDLER: Objection. Form. 10:54 | 16 Q. Is the content in that command truth table 11:17 |
| THE WITNESS: As I said, I'm not familiar 10:54 | 17 something that had a person of ordinary skill in the 11:17 |
| 18 off the top of my head with every JEDEC standard. 10:54 | 18 art would be familiar with at the time of the '912 11:17 |
| 19 But the particular example that's quoted in 10:54 | 19 inventions? 11:17 |
| 20 paragraph 133 that's from column 13, line 54, is 10:54 | 20 A. Yes. 11:18 |
| 21 describing something that's distinct from JESD21-C. 10:54 | 21 Q. So, for example, they would know, for a 11:18 |
| 22 BY MS. ZHONG: 10:54 | 22 DDR SDRAM, a write operation would include bank 11:18 |
| | _ |
| , 1 | 23 address information; is that correct? 11:18 |
| 24 paragraph 133 is a different signaling scheme than 10:54 | 24 A. Yes, for things that are compliant within 11:18 |
| 25 that is used for the RDIMM described in 10:54 Page 66 | 25 JEDEC Standard 79-2. 11:18 Page 68 |
| | |
| 1 Exhibit 1032; is that correct? 10:55 | 1 Q. So they would know that in order for the 11:18 |
| 2 A. It is not an identical signaling 10:55 | 2 SDRAM to perform a write operation the DIMM has to 11:18 |
| 3 mechanism, but it does have teachings that are 10:55 | 3 receive the bank address signals, correct? 11:18 |
| 4 applicable to the signaling mechanism used for DDR2. 10:55 | 4 A. Was the question that the DIMM has to 11:18 |
| 5 Q. Okay. So, for example, it does not have 10:55 | 5 receive the bank address signals? 11:18 |
| 6 the CS signal, the CAS, RAS let's go to page 16 10:55 | 6 Q. Correct. 11:18 |
| 7 of Exhibit 1032. 10:55 | 7 A. That's from JESD79-2, which does not 11:19 |
| 8 A. Uh-huh. 10:55 | 8 require a DIMM. But if that particular chip were on 11:19 |
| 9 Q. For example, the signaling scheme 10:55 | 9 a DIMM, then the DIMM would need to receive the bank 11:19 |
| 10 described in 133 would not have the signals that's 10:55 | 10 address signals. 11:19 |
| 11 listed on the left-hand side of the register box; is 10:55 | 11 Q. Okay. And so if a DDR or DDR2 device is 11:19 |
| 12 that correct? 10:56 | 12 on the DIMM, does that DIMM have to receive a bank 11:19 |
| 13 A. I think it would have those signals. It 10:56 | 13 address signal in order to perform a read operation? 11:19 |
| 14 just wouldn't necessarily have them in the exact 10:56 | 14 A. If you're using a JEDEC Standard 79-2 11:19 |
| 15 same physical form. It would have them in a way 10:56 | 15 memory on a DIMM, then that DIMM would need a bank 11:1 |
| 16 that has a different physical implementation. But 10:56 | 16 address signal. 11:19 |
| 17 certainly a person of ordinary skill in the art 10:56 | 17 Q. Are you aware of DRAMs that do not use 11:19 |
| 18 would understand how the teachings apply to both. 10:56 | 18 bank address signals for read or write operation? 11:19 |
| 19 Q. Okay. So they will be a different 10:56 | 19 A. Yes. 11:20 |
| 20 physical implementation that's different than what's 10:56 | 20 Q. Which kind of DRAMs do not use bank 11:20 |
| 21 described on Enhibit 1022 and 16 in that sinks 10.56 | 21 address signals for read and write operation? 11:20 |
| 21 described on Exhibit 1032, page 16; is that right? 10:56 | |
| 22 A. That's true with respect to that one 10:56 | 22 A. I'd have to go back and look at the 11:20 |
| | |
| A. That's true with respect to that one 10:56 23 particular statement. If you look at the teaching 10:56 | 23 specific specifications. But, based on my 11:20 |
| 22 A. That's true with respect to that one 10:56 23 particular statement. If you look at the teaching 10:56 | 23 specific specifications. But, based on my 11:20 |

| 1. Q. Okay. What about DDR2. DDR SDRAMs? Are 11-20 2 you ware of any such memory devices that do not use 11-20 3 bank address signals for read or write operation? 11-20 4 A. Thy DDR and DDR2 you mean things that 11-20 5 squestion, please 11-25 5 or are compliant with JESD79 or IESD79-2, in that cases 11-20 5 squestion, please 11-25 5 squestion, please 11-25 5 squestion, please 11-25 7 signal at the memory chip device itself. It doesn't 11-21 7 or a bond of the among the provided by the provided to may hing clean 11-21 7 or a bond of the post of may hing clean 11-21 7 or a bond of the SDRAM if the signal is not sent to 11-21 12 to bond the SDRAM if the signal is not sent to 11-21 13 or a bond of the SDRAM if the signal is not sent to 11-21 14 or a bond which the SDRAM is sent on the signal is not sent to 11-21 15 or a bond on the bunk address signals be 11-21 15 or a bond of the SDRAM if the signal is not sent to 11-21 15 or a bond on the solid on a devising. You could generate them on the 11-21 15 or a bond on the solid of inference ways. You 11-21 15 or a bond on the bond by the signal is not sent to 11-21 15 or a bond on the solid on a devising. You could generate them on the 11-21 15 or a bond on the solid on a devising. You could generate them on the 11-21 15 or a bond on the solid on a devising. You could generate them on the 11-21 15 or a bond on the person of the you, it is not 11-21 15 or a bond on the person of the you it, it is not 11-21 15 or a bond on the person of the you it, it is not 11-21 15 or a bond on the person of the you it, it is not 11-22 15 or a bond with the SDRAM is set on to receive a chip 11-22 15 or a bond with the SDRAM is set on to receive a chip 11-22 15 or a bond with the solid with the soli | | |
|--|---|--|
| 3 bank address signals for read or write operations 1120 4 A . If hy DDR and DDR2 you mean strings that 1120 4 Comset. Hot you on that one. Repert your 1125 126 6 Pm not aware of any that don't use a bank address 1120 5 Pm not aware of any that don't use a bank address 1120 5 Pm not aware of any that don't use a bank address 1120 5 Pm not aware of any that don't use a bank address 1120 5 Pm not aware of any that don't use a bank address 1121 121 121 121 122 12 Pm not aware of any that don't use a bank address 1121 12 | | |
| A. If by DDR and DDR2 you mean things that case 1120 5 are compliant with JRSD79 or JRSD79-2, in that case 1120 5 are compliant with JRSD79 or JRSD79-2, in that case 1120 5 are compliant with JRSD79 or JRSD79-2, in that case 1120 7 and JRSD79 or JRSD79-2, in that case 1120 7 and JRSD79-2 1120 7 and JRSD79-2 1120 7 and JRSD79-2 1120 7 and JRSD79-2 1120 1120 7 and JRSD79-2 1120 | 2 you aware of any such memory devices that do not use 11:20 | 2 art that DDR2 (indiscernible.) 11:24 |
| 5 are compliant with JESD79 or JESD79-2, in that case 11:20 | 3 bank address signals for read or write operation? 11:20 | 3 THE REPORTER: I'm sorry. Excuse me, 11:25 |
| 6 Pm not aware of any that don't use a bank address 11:20 7 8 8 9 8 12:20 7 8 9 8 12:20 7 8 8 8 12:20 7 9 9 9 12:20 12 | 4 A. If by DDR and DDR2 you mean things that 11:20 | 4 Counsel. I lost you on that one. Repeat your 11:25 |
| 1-21 | 5 are compliant with JESD79 or JESD79-2, in that case 11:20 | 5 question, please. 11:25 |
| 8 necessarily have to be provided to anything else on 11:21 9 the DIMM 11:21 11:21 10 DIMM on which the SDRAM if the signal is not sent to 11:21 11 12:11 12 13 DIMM on which the SDRAM is ent on? 11:21 12 14 could do a design. You could generate them on the 11:21 15 DIMM hypothetically, depending on what you were right of using the DIMM for and what you were rying to 11:21 15 DIMM hypothetically, depending on what you were rying to 11:21 15 DIMM hypothetically, depending on what you were rying to 11:21 15 DIMM hypothetically, depending on what you were rying to 11:21 15 DIMM hypothetically, depending on what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:25 15 DIMM for and what you were rying to 11:21 15 DIMM for and what you were rying to 11:26 15 DIMM for and what you were rying to 11:26 17 Such as chip select signals, would that also be 11:26 11:26 12:20 DIMM for and what you were rying to 11:26 12:20 DIMM for and what you were rying to 11:26 12:20 DIMM for and what you were rying to 11:26 12:20 DIMM for and what you were rying to 11:26 12:20 DIMM for and what you were rying to 11:26 12:20 DIMM for and what you were rying to 11:26 12:20 DIMM for and what you were rying to 11:26 DIMM for and what you were rying to 11:26 DIMM for and what you were rying to DIMM for any with the person of provided with the | 6 I'm not aware of any that don't use a bank address 11:20 | 6 BY MS. ZHONG: 11:25 |
| 9 the DIMM. | 7 signal at the memory chip device itself. It doesn't 11:21 | 7 Q. So in 2004 and 2005, when a person with 11:25 |
| 10 Q. So how can the bank address signals be 11:21 11 12 12 13 14 15 15 15 15 15 15 15 | 8 necessarily have to be provided to anything else on 11:21 | 8 ordinary skill in the art mentions a DRAM device, 11:25 |
| 11 provided to the SDRAM if the signal is not sent on? | 9 the DIMM. 11:21 | 9 would others understand that the DRAM device they 11:25 |
| 11-21 12 12 12 13 13 14 14 15 15 16 16 16 17 17 17 17 17 | 10 Q. So how can the bank address signals be 11:21 | 10 refer to would include DDR2 or DDR device? 11:25 |
| 13 | 11 provided to the SDRAM if the signal is not sent to 11:21 | 11 A. I think they would understand that it 11:25 |
| 14 could do a design. You could generate them on the 11:21 15 DMM hypothetically, depending on what you were 11:21 15 D. Okay. And if the person — the 11:26 11: | 12 the DIMM on which the SDRAM is sent on? 11:21 | 12 could include a DDR or DDR2 device, especially if 11:25 |
| 15 DIMM hypothetically, depending on what you were trying to 11:21 16 using the DIMM for and what you were trying to 11:21 17 accomplish. 11:21 18 Q. Okay. So according to you, it is not 11:21 18 Consistent with the reference to a DDR or DDR2 11:26 18 Consistent with the reference to a DDR or DDR2 11:26 11:26 12:20 20 address signals, RAS, CAS – let me withdraw and 11:22 19 device? 11:26 11:26 11:26 11:26 12:21 21 ask. 11:22 22 Is — would it also be the case that for a 11:22 23 Rad and write operation that's to be performed by a 11:22 23 Q. What do you mean by "ordinary" 11:26 11:27 11:26 11:27 11:28 11:28 11:29 11:2 | 13 A. There are lots of different ways. You 11:21 | 13 they were in the context of a general purpose 11:25 |
| 11-21 16 description for that DRAM device also include things 11-26 17 accomplish. 11-21 18 0.0 Okay. So according to you, it is not 11-21 18 0.0 Okay. So according to you, it is not 11-21 18 0.0 Okay. So according to you, it is not 11-21 18 0.0 Okay. So according to you, it is not 11-21 18 0.0 Okay. So according to you, it is not 11-21 18 0.0 Okay. So according to you, it is not 11-22 19 device? 11-26 11 | 14 could do a design. You could generate them on the 11:21 | 14 computer. 11:26 |
| 17 | 15 DIMM hypothetically, depending on what you were 11:21 | 15 Q. Okay. And if the person the 11:26 |
| 18 Q. Okay. So according to you, it is not 11:21 18 consistent with the reference to a DDR or DDR2 11:26 19 device? 11:26 12:26 20 address signals, RAS, CAS let me withdraw and 11:22 21 ask. 11:22 22 Is would it also be the case that for a 11:22 23 read and write operation that's to be performed by a 11:22 23 read and write operation that's to be performed by a 11:22 23 read and write operation that's to be performed by a 11:22 24 DDR, a DDR2 SDRAM, it is not necessary for the DIMM 11:22 25 read and write operation that's to be performed by a 11:22 25 read and write operation that's to be performed by a 11:22 25 read and write operation that's to be performed by a 11:22 25 read and write operation that's to be performed by a 11:22 25 read and write operation that's to be performed by a 11:22 25 read and write operation that is not necessary for the DIMM 11:23 26 read and write operation that is not necessary for the DIMM 11:23 27 read and write operation that is not necessary for the DIMM 11:23 28 read and write operation that is not necessary for the DIMM 11:23 29 read would in blood the necessary, but it would be 11:23 11:26 read and write operation that or receive a chip select signal. 11:27 read and write operation in the provided with a bank 11:23 11:28 11:29 1 | 16 using the DIMM for and what you were trying to 11:21 | 16 description for that DRAM device also include things 11:26 |
| 19 necessary for DIMM to receive, for example, bank 11:22 12 ask. 11:22 22 in the seed of chip select signals on a DDR or | 17 accomplish. 11:21 | 17 such as chip select signals, would that also be 11:26 |
| 20 address signals, RAS, CAS – let me withdraw and 11:22 21 ask. 11:22 22 Is – would it also be the case that for a 11:22 23 read and write operation that's to be performed by a 11:22 23 read and write operation that's to be performed by a 11:22 23 read and write operation that's to be performed by a 11:22 24 A. For the most commonly available devices 11:27 Page 70 11:26 11:27 Page 70 11:26 11:27 Page 71 11:28 11:29 Page 70 11:26 11:27 Page 72 11:26 11:27 Page 72 11:28 11:29 Page 70 11:28 11:29 Page 70 11:27 Page 72 11:28 11:29 Page 70 11:27 Page 72 Page 7 | 18 Q. Okay. So according to you, it is not 11:21 | 18 consistent with the reference to a DDR or DDR2 11:26 |
| 21 ask. 11:22 23 Is - would it also be the case that for a 11:22 24 DDR, a DDR2 SDRAM, it is not necessary for the DIMM 11:22 25 on which the SDRAM is set on to receive a chip 11:22 26 A. It would not be necessary, but it would be 11:22 27 A. It would not be necessary, but it would be 11:22 28 A. It would not be necessary, but it would be 11:22 39 C. And would it be ordinary for the DIMM to 11:23 40 SQL A. It would not be necessary, but it would be 11:22 41 Signal 11:26 42 JESDT9-2 and would include a chip select input. 11:27 43 ordinary for the DIMM to receive a chip select 11:22 44 Signal 11:22 55 Q. And would it be ordinary for the DIMM to 11:23 57 Q. And would it be ordinary for the DIMM to 11:23 58 A. If it were a memory DIMM that used memory 11:23 59 chips compliant with JESDT9 or JESDT9-2, it would be 11:23 61 cordinarily for that DIMM to be provided with a bank 11:23 62 simplest case, would go directly to the memory 11:23 63 devices. 11:23 64 Q. What if it is a registered DIMM? Would 11:23 65 that bank address signal go to the register on the 11:23 66 DIAM side then? 11:23 67 A. A. Again, we'd have to look at the particular 11:23 68 that bank address signal go to the register on the 11:23 69 JESD21-C registered DIMMS, bank address signals 11:23 70 Q. Weet DDR2 or DDR DRAMS common at the time 11:24 71 Q. Weet DDR2 or DDR DRAMS common at the time 11:24 72 Q. Weet DDR2 or DDR DRAMS common at the time 11:24 73 Q. Weet DR2 or DDR DRAMS common at the time 11:24 74 Q. Weet DR2 or DDR DRAMS common at the time 11:24 75 Q. Weet DR2 or DDR DRAMS common at the time 11:24 76 Q. Weet DR2 or DDR DRAMS common at the time 11:24 77 A. Again, we'd have to look at the particular 11:23 78 A. By "common" do you mean by "ordinary" in 11:26 79 C. And you said that if the DRAM device was 11:27 79 Lize Table Ta | 19 necessary for DIMM to receive, for example, bank 11:22 | 19 device? 11:26 |
| 22 Iswould it also be the case that for a 11:22 22 memory device is ordinary. 11:26 24 DDR, a DDR2 SDRAM, it is not necessary for the DIMM 11:22 24 A. For the most commonly available devices 11:27 25 would that are DDR or DDR2 in the 2004, 2005, 11:27 Page 70 Page 72 Page 72 Page 70 Page 70 Page 72 Page 70 Page 72 Page 70 Page 72 Page 70 Page 70 Page 70 Page 70 Page 70 Page 70 | 20 address signals, RAS, CAS let me withdraw and 11:22 | 20 A. If I understand your question correctly, 11:26 |
| 23 read and write operation that's to be performed by a 11:22 to DDR, a DDR2 SDRAM, it is not necessary for the DIMM 11:22 to m which the SDRAM is set on to receive a chip 11:22 to m which the SDRAM is set on to receive a chip 11:22 to m which the SDRAM is set on to receive a chip 11:22 to m which the SDRAM is set on to receive a chip 11:22 to m which the SDRAM is set on to receive a chip 11:22 to m which the SDRAM is set on to receive a chip select 11:22 to 2 because it is select signal? 11:22 to 2 because it is select signal? 11:22 to 2 because it is select signal in the ordinary for the DIMM to receive a chip select 11:22 to 2 because it is select signal. 11:22 to 3 ordinary for the DIMM to receive a chip select 11:23 to 3 ordinary for the DIMM to receive a chip select 11:23 to 3 ordinary for the DIMM to receive a chip select 11:23 to 3 ordinary for the DIMM to receive a chip select 11:23 to 3 ordinary for the DIMM to receive a chip select 11:23 to 4 including a chip select signal, would that indicate 11:27 to a person of ordinary skill in the art that device 11:27 to a person of ordinary skill in the art that device 11:27 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art that device 11:28 to a person of ordinary skill in the art would understand 11:28 to a person of ordinary skill in the art would understand 11:28 to a person of ordinary skill in the art would be 11:28 to a perso | 21 ask. 11:22 | 21 the use of chip select signals on a DDR or DDR2 11:26 |
| 24 DDR, a DDR2 SDRAM, it is not necessary for the DIMM 11:22 Page 70 11:22 Page 70 12 would that are DDR or DDR2 in the 2004, 2005, 11:27 Page 72 1. select signal? 11:22 1 2006 time frame would be compliant with JESD79 or 11:27 Page 72 1. select signal? 11:22 2 JESD79-2 and would include a chip select input. 11:27 3. ordinary for the DIMM to receive a chip select 11:22 3 Q. So if a DRAM device is described as 11:27 5. Q. And would it be ordinary for the DIMM to 11:23 4 including a chip select signal, would that indicate 11:27 6. receive a bank address signal for a read and write 11:23 5 to a person of ordinary skill in the art that device 11:27 7. operation? 11:23 6 is likely a DDR2 or DDR device? 11:27 9. chips compliant with JESD79 or JESD79-2, it would be 11:23 9 Q. And you said that if the DRAM device was 11:28 10 ordinarily for that DIMM to be provided with a bank 11:23 10 used in connection with a personal computer, then a 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would person 11:28 | 22 Is would it also be the case that for a 11:22 | 22 memory device is ordinary. 11:26 |
| 25 on which the SDRAM is set on to receive a chip Page 70 11:22 Page 70 1 select signal? 11:22 2 A. It would not be necessary, but it would be 11:22 3 ordinary for the DIMM to receive a chip select 11:22 4 signal. 11:22 4 signal. 11:22 5 Q. And would it be ordinary for the DIMM to 11:23 5 Q. And would it be ordinary for the DIMM to 11:23 6 receive a bank address signal for a read and write 11:23 7 operation? 11:23 8 A. If it were a memory DIMM that used memory 11:23 9 chips compliant with JESD79 or JESD79-2, it would be 11:23 11 address signal. That bank address signal, in the 11:23 12 simplest case, would go directly to the memory 11:23 12 simplest case, would go directly to the memory 11:23 13 devices. 11:23 14 Q. What if it is a registered DIMM? Would 11:23 15 that bank address signal go to the register on the 11:23 16 DIMM side then? 11:24 17 A. Again, we'd have to look at the particular 11:23 18 standards. But in the case of, for example, the 11:24 19 JESD21-C registered DIMMs, bank address signals 11:24 20 would go to a register typically. 11:24 21 Q. Were DDR2 or DDR SDRAMs common at the time 11:24 22 Of the '912 invention? 11:25 23 A. By "common" do you mean generally 11:24 24 available? 11:26 11:27 2 JESD79-2 and would include a chip select input. 11:27 11:27 2 JESD79-2 and would include a chip select input. 11:27 11:27 11:28 11:27 1 2 JESD79-2 and would include a chip select input. 11:27 11:27 11:27 1 2 JESD79-2 and would include a chip select input. 11:27 1 3 Q. So if a DRAM device is described as 11:27 11:27 1 4 including a chip select signal would that indicate 11:27 1 5 to a person of ordinary skill in the art that device 11:27 1 6 is likely a DDR2 or DDR device? 11:28 1 identifying or distinguishing characteristic. 11:28 1 ident | 23 read and write operation that's to be performed by a 11:22 | 23 Q. What do you mean by "ordinary"? 11:26 |
| Page 70 1 select signal? 11:22 2 A. It would not be necessary, but it would be 11:22 2 JESD79-2 and would include a chip select input. 11:27 3 ordinary for the DIMM to receive a chip select 11:22 4 signal. 11:22 4 signal. 11:23 5 Q. And would it be ordinary for the DIMM to 11:23 6 receive a bank address signal for a read and write 11:23 8 A. If it were a memory DIMM that used memory 11:23 9 chips compliant with JESD79 or JESD79-2, it would be 11:23 9 chips compliant with JESD79 or JESD79-2, it would be 11:23 10 ordinarily for that DIMM to be provided with a bank 11:23 11 address signal. That bank address signal, in the 11:23 12 simplest case, would go directly to the memory 11:23 13 devices. 11:23 12 What if it is a registered DIMM? Would 11:23 13 devices. 11:23 14 Q. What if it is a registered DIMM? Would 11:23 15 that bank address signal go to the register on the 11:23 16 DIMM side then? 17 A. Again, we'd have to look at the particular 11:23 18 standards. But in the case of, for example, the 11:23 19 JESD21-C registered DIMMs, bank address signals 11:24 10 would go to a register typically. 11:24 20 Were DDR2 or DDR SDRAMs common at the time 11:24 21 Q. Were DDR2 or DDR SDRAMs common at the time 11:24 22 Of the 912 invention? 11:25 12 supplest case, would go directly to the memory 11:23 13 correct? 14 A. That would be true in the 2000 to 2006 11:28 15 time frame. 11:28 16 Q. Okay. And then they would understand that 11:28 17 if those are DDR and DDR2 device, in order for the 11:29 18 standards. But in the case of, for example, the 11:23 19 JESD21-C registered DIMMs, bank address signals 11:29 10 would go to a register typically. 11:24 22 CAS bar, RAS bar, and write enable bar; is that 11:29 23 A. By "common" do you mean generally 11:24 24 A. It would be ordinary to send those to an 11:29 | 24 DDR, a DDR2 SDRAM, it is not necessary for the DIMM 11:2: | 2 24 A. For the most commonly available devices 11:27 |
| 2 A. It would not be necessary, but it would be 11:22 3 ordinary for the DIMM to receive a chip select 11:22 4 signal. 11:22 5 Q. And would it be ordinary for the DIMM to 11:23 5 Q. And would it be ordinary for the DIMM to 11:23 6 receive a bank address signal for a read and write 11:23 7 operation? 11:23 8 A. If it were a memory DIMM that used memory 11:23 9 chips compliant with JESD79 or JESD79-2, it would be 11:23 10 ordinarily for that DIMM to be provided with a bank 11:23 11 address signal. That bank address signal, in the 11:23 12 simplest case, would go directly to the memory 11:23 13 devices. 11:23 14 Q. What if it is a registered DIMM? Would 11:23 15 that bank address signal go to the register on the 11:23 16 DIMM side then? 11:23 17 A. A. Again, we'd have to look at the particular 11:23 18 standards. But in the case of, for example, the 11:23 19 JESD21-C registered DIMMs, bank address signals 11:24 20 would go to a register typically. 11:24 21 Q. Were DDR2 or DDR SDRAMs common at the time 11:24 22 of the '912 invention? 11:24 23 A. By "common" do you mean generally 11:24 24 available? 11:24 24 JESD79-2 and would include a chip select input. 11:27 3 Q. So if a DRAM device is described as 11:27 4 including a chip select signal, would that indicate 11:27 5 to a person of ordinary skill in the art that device 11:27 6 is likely a DDR2 or DDR device? 11:28 8 identifying or distinguishing characteristic. 11:28 8 identifying or distinguishing characteristic. 11:28 9 Q. And you said that if the DRAM device was 11:28 10 used in connection with a personal computer, then a 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 12 that a DRAM device could be a DDR2 or DDR device, 11:28 13 correct? 11:28 14 A. That would be true in the 2000 to 2006 11:28 15 time frame. 11:28 16 Q. Okay. And then they would understand that 11:29 17 those are DDR and DDR2 device, in order for the 11:29 18 DDR in order for the memory device to perform a 11:2 | 1 | |
| 3 ordinary for the DIMM to receive a chip select 11:22 | 1 select signal? 11:22 | 1 2006 time frame would be compliant with JESD79 or 11:27 |
| 4 signal. 11:22 5 Q. And would it be ordinary for the DIMM to 11:23 6 receive a bank address signal for a read and write 11:23 7 operation? 11:23 8 A. If it were a memory DIMM that used memory 11:23 9 chips compliant with JESD79 or JESD79-2, it would be 11:23 10 ordinarily for that DIMM to be provided with a bank 11:23 11 address signal. That bank address signal, in the 11:23 12 simplest case, would go directly to the memory 11:23 13 devices. 11:23 14 Q. What if it is a registered DIMM? Would 11:23 15 that bank address signal go to the register on the 11:23 16 DIMM side then? 11:23 17 A. Again, we'd have to look at the particular 11:23 18 standards. But in the case of, for example, the 11:23 19 JESD21-C registered DIMMs, bank address signals 11:24 20 would go to a register typically. 11:24 21 Q. Were DDR2 or DDR SDRAMs common at the time 11:24 22 CAS bar, RAS bar, and write enable bar; is that 11:29 24 available? 11:24 4 including a chip select signal, would that indicate 11:27 5 to a person of ordinary skill in the art that device 11:27 6 is likely a DDR2 or DDR device? 11:27 7 A. No, that would generally not be a 11:28 8 identifying or distinguishing characteristic. 11:28 10 used in connection with a personal computer, then a 11:28 11 person of ordinary skill in the art that device was 11:28 10 used in connection with a personal computer, then a 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of ordinary skill in the art would understand 11:28 11 person of | 2 A. It would not be necessary, but it would be 11:22 | 2 JESD79-2 and would include a chip select input. 11:27 |
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| 18 standards. But in the case of, for example, the 11:23 | 16 DIMM side then? | |
| 19 JESD21-C registered DIMMs, bank address signals 11:23 19 read, write, bank activation operation, it would be 20 would go to a register typically. 11:24 20 ordinary for the computer system to send signals 11:29 21 Q. Were DDR2 or DDR SDRAMs common at the time 11:24 21 such as bank address signals, chip select signals, 11:29 22 of the '912 invention? 11:24 22 CAS bar, RAS bar, and write enable bar; is that 11:29 23 A. By "common" do you mean generally 11:24 23 correct? 11:29 24 available? 11:24 24 A. It would be ordinary to send those to an 11:29 | 17 A. Again, we'd have to look at the particular 11:23 | |
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| 24 available? 11:24 24 A. It would be ordinary to send those to an 11:29 | | |
| | 23 A. By "common" do you mean generally 11:24 | |
| | 24 available? 11:24 | - |
| | | 25 ordinary personal computer in DDR or DDR2 module at 11:29 Page 73 |

| 1 that time. 11:30 | 1 Q. In the Rambus memory module that you are 11:34 |
|--|---|
| 2 Q. What do you mean by "It would be ordinary 11:30 | |
| | 1 |
| 3 to send those to an ordinary personal computer in 11:30 | |
| 4 DDR or DDR2 module"? 11:30 | 4 A. There is not a distinct chip select bus. 11:34 |
| 5 A. One could one can use these chips in 11:30 | 5 It's subsumed into the into the Rambus channel. 11:34 |
| 6 many different ways and build many different kinds 11:30 | 6 Q. And what's your understanding of the chip 11:35 |
| 7 of memory modules. But there were typical memory 11:30 | 7 select bus in the context of Exhibit 1034? 11:35 |
| 8 modules at the time that were JEDEC compliant with 11:30 | 8 A. I think that it's simply saying that in a 11:35 |
| 9 various JEDEC standards. 11:30 | 9 conventional PC-type memory system as of 2002 and 11:35 |
| Q. Are you saying those CAS bar, RAS bar, WE, 11:30 | 10 by "conventional," that's not the Rambus type 11:35 |
| 11 and chip select and bank address signals are sent to 11:30 | 11 that there is a chip select signal provided for 11:35 |
| 12 the personal computer instead of being sent from the 11:30 | 12 every rank of memory in order to control the timing 11:35 |
| 13 personal computer to the memory modules? 11:30 | 13 of that rank with respect to responding to commands. 11:35 |
| MR. CHANDLER: Vague. 11:31 | 14 Q. So what's the difference between a bus 11:35 |
| THE WITNESS: No. 11:31 | 15 versus the point-to-point architecture described in 11:36 |
| 16 BY MS. ZHONG: 11:31 | 16 Perego? 11:36 |
| 17 Q. Hello? 11:31 | 17 A. A bus can be used broadly here. I think 11:36 |
| 11:31 | 18 in this particular reference, I think "bus" simply 11:36 |
| 9 Q. You are saying that it would be ordinary 11:31 | 19 is being used to refer to a collection of wires. 11:36 |
| 20 for a personal computer to send CAS bar, RAS bar, WE 11:31 | 20 The again, and Perego does disclose 11:36 |
| 21 bar, chip select signals and bank address signals to 11:31 | 21 buses as alternatives to point-to-point. It 11:36 |
| 22 the memory module for a read and write operation at 11:31 | 22 discloses both kinds of embodiments numerous times. 11:36 |
| 23 the time of the invention; is that correct? 11:31 | 23 But in his point-to-point description in 11:36 |
| 24 A. Yes, I think that's fair. And then one 11:31 | 24 Perego, he talks about things that have one 11:36 |
| 25 would have to look at how those are then connected 11:32 Page 7- | 25 transceiver on each end, where in Perego buses used 11:36 Page 7 |
| 1 on the memory module to figure out whether or not 11:32 | 1 a thing described things that can have more than 11:36 |
| 2 that's at all relevant to these claims. 11:32 | 2 one transceiver. 11:36 |
| 3 Q. Is that something a person of ordinary 11:32 | 3 I'm not sure that it's being used in 11:36 |
| 4 skill in the art would understand? 11:32 | 4 exactly the same way here. It's quite possible 11:36 |
| 5 A. Yes. 11:32 | 5 that that this particular chip select bus the way 11:36 |
| 6 Q. Can you pull up Exhibit 1034. 11:33 | 6 it would normally be implemented would be 11:36 |
| 7 (Exhibit 1034 was marked for 11:33 | 7 point-to-point. 11:37 |
| 8 identification and attached 11:33 | 8 And it's also common to use the term "bus" 11:37 |
| 9 hereto.) 11:33 | 9 to simply refer to a collection of wires. And I 11:37 |
| 0 THE WITNESS: Okay. 11:33 | 10 believe that's what's being done in 1034 in the area 11:37 |
| 1 BY MS. ZHONG: 11:33 | 11 that we referred to. 11:37 |
| 2 Q. Can you please go to page 2 of 11:33 | 12 Q. Okay. So in the 2004 and 2005 time 11:37 |
| 13 Exhibit 1034. 11:33 | 13 period, a conventional PC system would send chip 11:37 |
| 4 A. Okay. 11:33 | 14 select signals, CAS bar, RAS bar, write enable bar, 11:37 |
| Q. The last paragraph on the right hand, 11:33 | 15 clock, bank address signals to a DIMM; is that 11:37 |
| 6 "disables the chip select bus." Do you see that? 11:33 | 16 correct? 11:37 |
| 17 A. Yes. 11:33 | 17 A. I don't know if it would send all of 11:37 |
| 8 Q. So according to this paper, the chip 11:33 | 18 those. 11:37 |
| 19 select bus is essential in the JEDEC-style memory 11:34 | 19 Q. Which signals you don't think it would 11:37 |
| 20 system. Do you agree with that? 11:34 | 20 send? 11:38 |
| 21 A. In the context that's being used in this 11:34 | 21 A. I don't think it's just a clock at that 11:38 |
| 22 paper where it's talking about DIMMs in a 11:34 | 22 time frame. I think it tends to be a little more 11:38 |
| 23 traditional computer, I do think that the chip 11:34 | 23 complicated, and there are a number of 11:38 |
| 24 select bus is essential in as far as it needs to 11:34 | 24 Q. Okay. 11:38 |
| | |
| 25 exist. 11:34 | 25 A timing signals that are sent. 11:38 |